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Docket No.: 02008/135001
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Letters Patent of:
Masaru Doi et al.

Patent No.: 7,283,920

Issued: October 16, 2007

For: APPARATUS AND METHOD FOR TESTING
_____SEMICONDUCTOR DEVICE

REQUEST FOR CERTIFICATE OF CORRECTION
PURSUANT TO 37 CFR 1.322

Attention: Certificate of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Upon reviewing the above-identified patent, Patentee noted typographical errors which should be corrected.

In the Drawings:

In the drawings, sheet 24 of 28, figure number 25 is incorrect. Please replace the drawing with the replacement drawing enclosed.

In the Claims:

In Claim 12, column 29, line 27, the word "An" should be deleted.

In Claim 21, column 31, line 4, the word "An" should be deleted.

In Claim 35, column 33, line 55, the word "whereiii" should be --**wherein**--.

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In Claim 38, column 34, line 10, the word "riot" should be --**not**--.

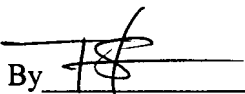In Claim 38, column 34, line 11, the word "astrobe" should be --**a strobe**--.

The errors were not in the application as filed by applicant; accordingly no fee is required.

Transmitted herewith is a proposed Certificate of Correction effecting such amendment. Also enclosed, as evidence of the error, is a copy of Fig. 25 as issued; a copy of the Replacement Sheet for Fig. 25 filed on December 5, 2006; a copy of the claims as issued; and pages 2-15 of the Amendments to the Claims. Patentee respectfully solicits the granting of the requested Certificate of Correction.

Applicant believes no fee is due with this request. However, if a fee is due, please charge our Deposit Account No. 50-0591, under Order No. 02008/135001.

Dated: November 8, 2007   Respectfully submitted,

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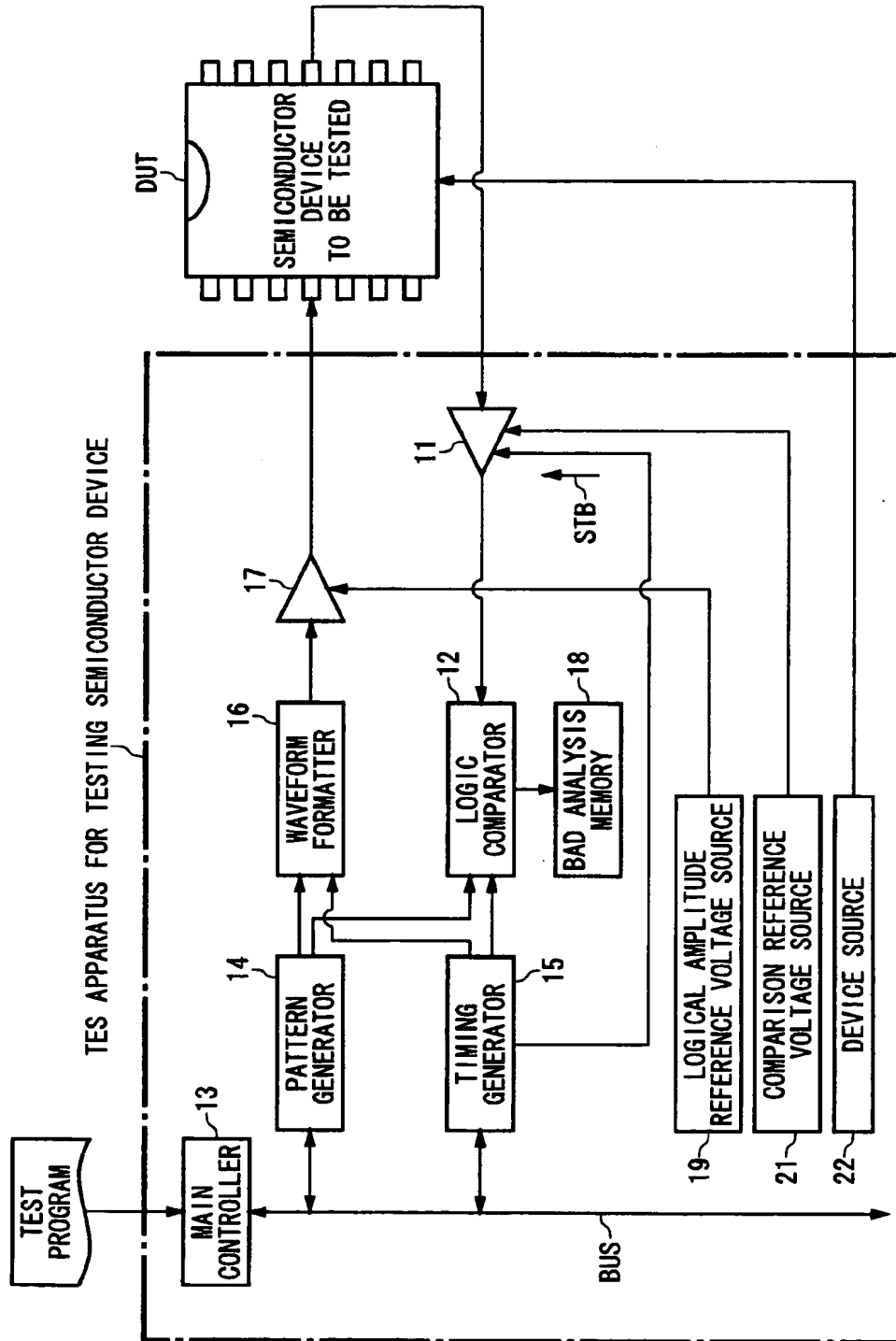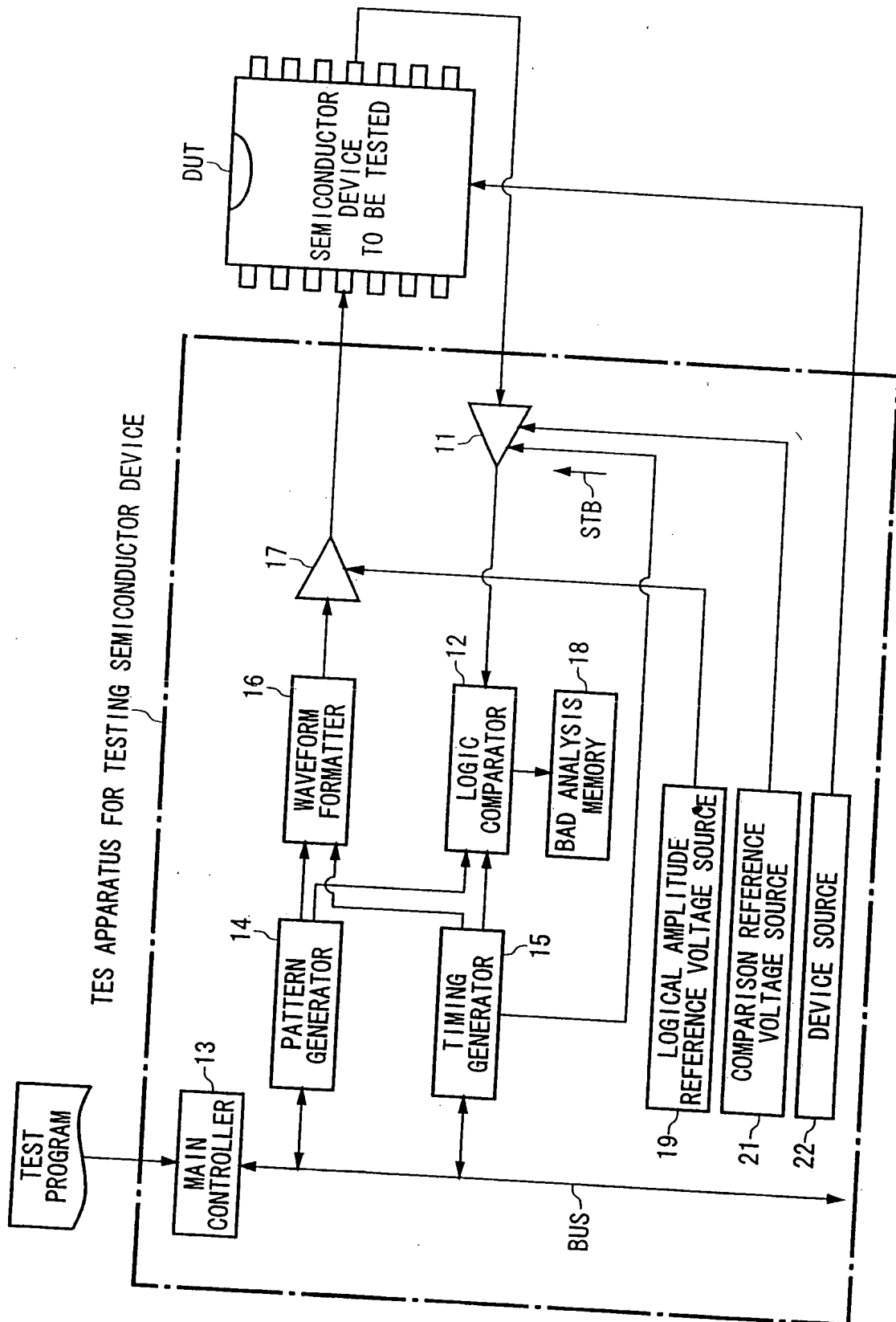(713) 228-8600
(713) 228-8778 (Fax)

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FIG. 25

FIG. 25
(Prior Art)

TEST APPARATUS FOR TESTING SEMICONDUCTOR DEVICE

using the judging unit 110 described in relation to FIG. 9 if there is no glitch of the output data.

According to the method for testing a semiconductor device described above, it is possible to detect the rising or falling of the waveform of the output data and the reference clock DQS, and thus the test can be performed effectively. In addition, it is possible to easily detect the existence of the glitch in regard to the output data, and therefore the test can be performed with more high accuracy.

FIG. 24 shows a flowchart of another embodiment of a method for testing a semiconductor device relating to the present invention. First, in a reference phase measuring step, the output timing of the reference clock is measured (S202). In S202, the output timing of the reference clock may be measured by using, for example, the reference phase measuring unit 172 described in relation to FIG. 2.

Then, in a reference phase memorizing step, the output timing measured is memorized (S204). In S204, the output timing may be measured by using, for example, the memory 32 described in relation to FIG. 2.

Then, in a first multi-strobe generating step, the first multi-strobe having a plurality of strobes, of which the phases are different by a small amount, is generated for the output data of a semiconductor device (S206). In S206, the first multi-strobe may be generated by using, for example, the first multi-strobe generator 34 described in relation to FIG. 2 or the first multi-strobe generator 154 described in relation to FIG. 18.

Then, in an output data transition point detecting step, the timing of rising or falling of the waveform of the output data is detected based on the first multi-strobe (S208). In S208, the timing of rising or falling of the waveform of the output data may be detected by using, for example, the output data transition point detector 142 described in relation to FIG. 18.

Then, in a phase difference measuring step, the phase difference between the output timing of the reference clock DQS and the transition point of the value of the output data is measured (S210). In S210, the phase difference may be measured by using, for example, the logic comparator 12 described in relation to FIG. 2.

Then, in a glitch detecting step, the existence of the glitch in regard to the output data is detected based on the transition point of the value of the output data (S212). In S212, the existence of the glitch may be detected by using, for example, the detector 146 described in relation to FIG. 18.

Then, in a judging step, the quality of the semiconductor device is judged based on the existence of the glitch detected in the glitch detecting step S212 and the phase difference measured in S210 (S214). For example, in S214, the quality of the semiconductor device may be judged in the same method as the judging step described in relation to FIG. 23.

According to the method for testing a semiconductor device described above, it is possible to detect the rising or falling of the waveform of the output data and the reference clock DQS in a considerably short time, and thus the test can be performed effectively. In addition, it is possible to easily detect the existence of the glitch in regard to the output data, and therefore the test can be performed with high accuracy.

Although the present invention has been described by way of exemplary embodiments, it should be understood that those skilled in the art might make many changes and substitutions without departing from the spirit and the scope of the present invention, which is defined only by the appended claims.

As obvious from the description above, according to the present invention, it is possible to detect the timing of rising

or falling of the waveform of the output data and the reference clock DQS of the semiconductor device in a considerably short time, and to calculate the phase difference of the output data and the reference clock. Due to this, it is possible to perform the test effectively. In addition, it is possible to easily detect the existence of the glitch, and therefore the test can be performed with high accuracy.

What is claimed is:

1. An apparatus for testing a semiconductor device based on output data of said semiconductor device, comprising:

a multi-strobe generator configured to generate a multi-strobe having a plurality of strobes, of which phases are different by a small amount;

an output data transition point detector configured to detect a timing of rising or falling of a waveform of said output data based on said multi-strobe;

a reference clock transition point detector configured to detect a timing of rising or falling of a reference clock outputted by said semiconductor device accompanying said output data, wherein said reference clock is a signal to set a timing of passing said output data, based on said multi-strobe;

a judging unit configured to judge quality of said semiconductor device based on said timing of a timing of rising or falling of a waveform of said output data detected by said output data transition point detector and said timing of rising or falling of a waveform of said reference clock detected by said reference clock transition point detector; and

a glitch detector configured to detect existence of a glitch in regard to said output data based on said timing of rising or falling of a waveform of said output data detected by said output data transition point detector.

2. The apparatus for testing a semiconductor device as claimed in claim 1, wherein said judging unit judges quality of said semiconductor device based on whether or not a phase difference between said timing of rising or falling of a waveform of said output data detected by said output data transition point detector and said timing of rising or falling of a waveform of said reference clock detected by said reference clock transition point detector is within a predetermined range.

3. The apparatus for testing a semiconductor device as claimed in claim 1, wherein said multi-strobe generator generates a first multi-strobe in order to detect a transition point of a value of said output data and a second multi-strobe in order to detect a transition point of a value of said reference clock.

4. The apparatus for testing a semiconductor device as claimed in claim 3, further comprising a level comparator configured to change said output data and said reference clock into digital data represented by H logic or L logic, wherein

said output data transition point detector detects a value of said output data changed into said digital data in regard to a phase of each of strobes of said first multi-strobe, and if a value of said output data in regard to a phase of a first strobe of said first multi-strobe and a value of said output data in regard to a phase of a second strobe adjacent to said first strobe are different then determines said phase of said first strobe as said transition point of said value of said output data,

said reference clock transition point detector detects a value of said reference clock changed into said digital data in regard to a phase of each of strobes of said second multi-strobe, and if a value of said reference clock in regard to a phase of a third strobe of said

second multi-strobe and a value of said reference clock in regard to a phase of a fourth strobe adjacent to said third strobe are different then determines said phase of said third strobe as said transition point of said value of said reference clock, and

said judging unit judges quality of said semiconductor device based on said transition point of said value of said output data and said transition point of said value of said reference clock.

5. The apparatus for testing a semiconductor device as claimed in claim 4, wherein said judging unit judges quality of said semiconductor device based on whether or not a difference between a strobe number of said first multi-strobe indicating which timing of a strobe of said first multi-strobe said output data transition point detector detects said transition point of a value of said output data and a strobe number of said second multi-strobe indicating which timing of a strobe of said second multi-strobe said reference clock transition point detector detects said transition point of a value of said reference clock at is within a predetermined range.

6. The apparatus for testing a semiconductor device as claimed in claim 4, wherein said judging unit comprises a memory configured to store a reference table to set quality of said semiconductor device about a combination of said strobe number of said first multi-strobe, in which said transition point of a value of said output data is detected and said strobe number of said second multi-strobe, in which said transition point of a value of said reference clock is detected, and judges quality of said semiconductor device based on said reference table.

7. The apparatus for testing a semiconductor device as claimed in claim 4, wherein said output data transition point detector comprises means for detecting whether a value of digital data in regard to said transition point of a value of said output data changes from said H logic to said L logic or changes from said L logic to said H logic.

8. The apparatus for testing a semiconductor device as claimed in claim 7, wherein the apparatus further comprises a memory and stores a result of the glitch detector in the memory in association with said transition point of a value of said output data.

9. The apparatus for testing a semiconductor device as claimed in claim 4, wherein said output data transition point detector takes a transition point of an earliest phase or a transition point of a latest phase as said transition point of a value of said output data if a plurality of said transition points of a value of said output data are detected.

10. The apparatus for testing a semiconductor device as claimed in claim 1, wherein said judging unit judges quality of said semiconductor device further based on existence of said glitch detected by said glitch detector.

11. The apparatus for testing a semiconductor device as claimed in claim 1, wherein said glitch detector detects existence of a glitch in regard to said output data based on said transition point of a value of said output data.

12. An The apparatus for testing a semiconductor device as claimed in claim 11, wherein said glitch detector judges that there is said glitch of said output data if said transition points of a value of said output data are more than or equal to two.

13. The apparatus for testing a semiconductor device as claimed in claim 1, wherein said multi-strobe generator comprises a plurality of delay devices having different delay times, supplies a strobe to each of said plurality of delay devices and outputs a plurality of strobes, delayed to have a

different time delay respectively and outputud by said plurality of delay devices, as said multi-strobe.

14. The apparatus for testing a semiconductor device as claimed in claim 13, wherein said multi-strobe generator comprises a plurality of delay devices connected in cascade, supplies a strobe to each of said plurality of delay devices connected in cascade and generates said multi-strobe based on strobes delayed respectively and outputted by said plurality of delay devices.

15. The apparatus for testing a semiconductor device as claimed in claim 1, wherein the apparatus further comprises a memory and stores a result of the glitch detector in the memory in association with said transition point of a value of said output data.

16. An apparatus for testing a semiconductor device based on output data of said semiconductor device, comprising:

a first multi-strobe generator configured to generate a first multi-strobe having a plurality of strobes, of which phases are different by a small amount in regard to said output data;

a reference phase measuring unit configured to measure an output timing being a timing of rising or falling of a waveform of a reference clock which is a signal to set a timing of passing said output data and is outputted by said semiconductor device accompanied by said output data;

a reference phase memory configured to memorize said output timing;

a transition point detector for detecting a transition point of a value of said output data based on said first multi-strobe;

a phase difference measuring unit configured to measure a phase difference between said output timing and said transition point of a value of said output data;

a judging unit configured to judge quality of said semiconductor device based on said phase difference; and

a glitch detector configured to detect existence of a glitch in regard to said transition point of a value of said output data.

17. The apparatus for testing a semiconductor device as claimed in claim 16, wherein said transition point detector comprises means for changing said output data into digital data represented by H logic or L logic, and

said transition point detector detects a value of said output data in regard to a phase of each of strobes of said first multi-strobe, and if a value of digital data in regard to a phase of a first strobe of said first multi-strobe and a value of digital data in regard to a phase of a second strobe adjacent to said first strobe are different then determines said phase of said first strobe as said transition point of said value of said output data.

18. The apparatus for testing a semiconductor device as claimed in claim 17, wherein said transition point detector comprises means for detecting whether said value of digital data in regard to said transition point changes from said H logic to said L logic or changes from said L logic to said H logic.

19. The apparatus for testing a semiconductor device as claimed in claim 18, wherein said transition point detector takes a transition point of an earliest phase or a transition point of a latest phase as said transition point of a value of said output data if a plurality of said transition points of a value of said output data is detected.

20. The apparatus for testing a semiconductor device as claimed in claim 18, wherein the apparatus further com-

prises a memory and stores a result of the glitch detector in the memory in association with said transition point of a value of said output data.

21. An The apparatus for testing a semiconductor device as claimed in claim 16, wherein said reference phase measuring unit comprises:

means for generating a second multi-strobe having a plurality of strobes, of which phases are different by a small amount, in regard to said reference clock;

means for detecting said transition point of a value of said reference clock based on said second multi-strobe; and

means for calculating said output timing of said reference clock based on a strobe number of said second multi-strobe, in which said transition point of a value of said reference clock is detected.

22. The apparatus for testing a semiconductor device as claimed in claim 21, wherein said reference phase memory stores said strobe number of said second multi-strobe, in which said transition point of a value of said reference clock is detected.

23. The apparatus for testing a semiconductor device as claimed in claim 22, wherein said first multi-strobe generator sets a phase of said first multi-strobe based on said strobe number of said second multi-strobe stored by said reference phase memory.

24. The apparatus for testing a semiconductor device as claimed in claim 16, wherein said judging unit judges quality of said semiconductor device further based on existence of said glitch detected by said glitch detector.

25. The apparatus for testing a semiconductor device as claimed in claim 16, wherein said glitch detector judges that there is said glitch of said output data if said transition points of a value of said output data detected by said transition point detector are more than or equal to two.

26. The apparatus for testing a semiconductor device as claimed in claim 16, wherein said first multi-strobe generator comprises a plurality of delay devices connected in cascade, supplies a strobe to said plurality of delay devices connected in cascade, and generates said first multi-strobe based on strobes delayed respectively and outputted by said plurality of delay devices.

27. The apparatus for testing a semiconductor device as claimed in claim 16, wherein the apparatus further comprises a memory and stores a result of the glitch detector in the memory in association with said transition point of a value of said output data.

28. A method for testing a semiconductor device based on output data of said semiconductor device, comprising:

a first multi-strobe generating step of generating a first multi-strobe having a plurality of strobes, of which phases are different by a small amount, in regard to said output data;

an output data transition point detecting step of detecting a timing of rising or falling of a waveform of said output data based on said first multi-strobe;

a second multi-strobe generating step of generating a second multi-strobe having a plurality of strobes, of which phases are different by a small amount, in regard to a reference clock, which is a signal to set a timing of passing said output data, said reference clock being outputted by said semiconductor device accompanying said output data;

a reference clock transition point detecting step of detecting a timing of rising or falling of a waveform of said reference clock based on said second multi-strobe;

a judging step of judging quality of said semiconductor device based on said timing of rising or falling of a

waveform of said output data detected in said output data transition point detecting step and said timing of rising or falling of a waveform of said reference clock detected in said reference clock transition point detecting step;

an outputting step of outputting said judging quality of said semiconductor device; and

a glitch detecting step of detecting existence of a glitch in regard to said output data based on said transition point of a value of said output data,

wherein said judging step judges quality of said semiconductor device further based on existence of said glitch detected in said glitch detecting step.

29. The apparatus for testing a semiconductor device as claimed in claim 28, wherein the apparatus further comprises a memory and stores a result of the glitch detector in the memory in association with said transition point of a value of said output data.

30. A method for testing a semiconductor device based on output data of said semiconductor device, comprising:

a reference phase measurement step of measuring an output timing of a reference clock, which is a signal to set a timing of passing said output data, said reference clock being outputted by said semiconductor device accompanying said output data;

a reference phase memorizing step of memorizing said output timing;

a first multi-strobe generating step of generating a first multi-strobe having a plurality of strobes, of which phases are different by a small amount, in regard to said output data;

an output data transition point detecting step of detecting said transition point of a value of said output data based on said first multi-strobe;

a phase difference measuring step of measuring a phase difference between said output timing and said transition point of a value of said output data;

a judging step of judging quality of said semiconductor device based on said phase difference;

an outputting step of outputting said judging quality of said semiconductor device; and

a glitch detecting step of detecting existence of a glitch in regard to said output data based on said transition point of a value of said output data.

31. The apparatus for testing a semiconductor device as claimed in claim 30, wherein the apparatus further comprises a memory and stores a result of the glitch detector in the memory in association with said transition point of a value of said output data.

32. An apparatus for testing a semiconductor device based on output data of said semiconductor device, comprising:

a multi-strobe generator configured to generate a multi-strobe having a plurality of strobes, of which phases are different by a small amount;

an output data transition point detector configured to detect a timing of rising or falling of a waveform of said output data based on said multi-strobe;

a reference clock transition point detector configured to detect a timing of rising or falling of a reference clock outputted by said semiconductor device accompanying said output data, wherein said reference clock is a signal to set a timing of passing said output data, based on said multi-strobe;

a judging unit configured to judge quality of said semiconductor device based on said timing of a timing of rising or falling of a waveform of said output data detected by said output data transition point detector

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and said timing of rising or falling of a waveform of said reference clock detected by said reference clock transition point detector;

a level comparator configured to change said output data and said reference clock into digital data represented by H logic or L logic,

wherein said multi-strobe generator generates a first multi-strobe in order to detect a transition point of a value of said output data and a second multi-strobe in order to detect a transition point of a value of said reference clock,

wherein said output data transition point detector detects a value of said output data changed into said digital data in regard to a phase of each of strobes of said first multi-strobe, and if a value of said output data in regard to a phase of a first strobe of said first multi-strobe and a value of said output data in regard to a phase of a second strobe adjacent to said first strobe are different then determines said phase of said first strobe as said transition point of said value of said output data,

wherein said reference clock transition point detector detects a value of said reference clock changed into said digital data in regard to a phase of each of strobes of said second multi-strobe, and if a value of said reference clock in regard to a phase of a third strobe of said second multi-strobe and a value of said reference clock in regard to a phase of a fourth strobe adjacent to said third strobe are different then determines said phase of said third strobe as said transition point of said value of said reference clock,

wherein said judging unit judges quality of said semiconductor device based on said transition point of said value of said output data and said transition point of said value of said reference clock, and

wherein said output data transition point detector takes a transition point of an earliest phase or a transition point of a latest phase as said transition point of a value of said output data if a plurality of said transition points of a value of said output data are detected.

33. The apparatus for testing a semiconductor device as claimed in claim 32, wherein said multi-strobe generator comprises a plurality of delay devices having different delay times, supplies a strobe to each of said plurality of delay devices and outputs a plurality of strobes, delayed to have a different time delay respectively and outputted by said plurality of delay devices, as said multi-strobe.

34. The apparatus for testing a semiconductor device as claimed in claim 33, wherein said multi-strobe generator comprises a plurality of delay devices connected in cascade, supplies a strobe to each of said plurality of delay devices connected in cascade and generates said multi-strobe based on strobes delayed respectively and outputted by said plurality of delay device.

35. The apparatus for testing a semiconductor device as claimed in claim 32, whereiii said output data transition point detector comprises means for detecting whether a value of digital data in regard to said transition point of a value of said output data changes from said H logic to said L logic or changes from said L logic to said H logic.

36. The apparatus for testing a semiconductor device as claimed in claim 35, wherein the apparatus further comprises a memory and stores a result of the glitch detector in the memory in association with said transition point of a value of said output data.

37. The apparatus for testing a semiconductor device as claimed in claim 32, wherein said judging unit judges quality of said semiconductor device based on whether or

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not a phase difference between said timing of rising or falling of a waveform of said output data detected by said output data transition point detector and said timing of rising or falling of a waveform of said reference clock detected by said reference clock transition point detector is within a predetermined range.

38. The apparatus for testing a semiconductor device as claimed in claim 32, wherein said judging unit judges quality of said semiconductor device based on whether or not a difference between a strobe number of said first multi-strobe indicating which timing of a strobe of said first multi-strobe said output data transition point detector detects said transition point of a value of said output data and a strobe number of said second multi-strobe indicating which timing of a strobe of said second multi-strobe said reference clock transition point detector detects said transition point of a value of said reference clock at is within a predetermined range.

39. The apparatus for testing a semiconductor device as claimed in claim 32, wherein said judging unit comprises a memory configured to store a reference table to set quality of said semiconductor device about a combination of said strobe number of said first multi-strobe, in which said transition point of a value of said output data is detected and said strobe number of said second multi-strobe, in which said transition point of a value of said reference clock is detected, and judges quality of said semiconductor device based on said reference table.

40. The apparatus for testing a semiconductor device as claimed in claim 32, further comprising a glitch detector configured to detect existence of a glitch in regard to said output data based on said timing of rising or falling of a waveform of said output data detected by said output data transition point detector.

41. The apparatus for testing a semiconductor device as claimed in claim 40, wherein said judging unit judges quality of said semiconductor device further based on existence of said glitch detected by said glitch detector.

42. The apparatus for testing a semiconductor device as claimed in claim 40, wherein said glitch detector detects existence of a glitch in regard to said output data based on said transition point of a value of said output data.

43. The apparatus for testing a semiconductor device as claimed in claim 42, wherein said glitch detector judges that there is said glitch of said output data if said transition points of a value of said output data are more than or equal to two.

44. The apparatus for testing a semiconductor device as claimed in claim 40, wherein the apparatus further comprises a memory and stores a result of the glitch detector in the memory in association with said transition point of a value of said output data.

45. An apparatus for testing a semiconductor device based on output data of said semiconductor device, comprising:

a first multi-strobe generator configured to generate a first multi-strobe having a plurality of strobes, of which phases are different by a small amount in regard to said output data;

a reference phase measuring unit configured to measure an output timing being a timing of rising or falling of a waveform of a reference clock which is a signal to set a timing of passing said output data and is outputted by said semiconductor device accompanied by said output data;

a reference phase memory configured to memorize said output timing;

a transition point detector configured to detect a transition point of a value of said output data based on said first multi-strobe;

a phase difference measuring unit configured to measure a phase difference between said output timing and said transition point of a value of said output data; and

a judging unit configured to judge quality of said semiconductor device based on said phase difference,

wherein said transition point detector comprises means for changing said output data into digital data represented by H logic or L logic, and said transition point detector detects a value of said output data in regard to a phase of each of strobes of said first multi-strobe, and if a value of digital data in regard to a phase of a first strobe of said first multi-strobe and a value of digital data in regard to a phase of a second strobe adjacent to said first strobe are different then determines said phase of said first strobe as said transition point of said value of said output data,

wherein said transition point detector comprises means for detecting whether said value of digital data in regard to said transition point changes from said H logic to said L logic or changes from said L logic to said H logic, and

wherein said transition point detector takes a transition point of an earliest phase or a transition point of a latest phase as said transition point of a value of said output data if a plurality of said transition points of a value of said output data is detected.

46. The apparatus for testing a semiconductor device as claimed in claim 45, wherein the apparatus further comprises a memory and stores a result of the glitch detector in the memory in association with said transition point of a value of said output data.

47. The apparatus for testing a semiconductor device as claimed in claim 45, further comprising a glitch detector configured to detect existence of a glitch in regard to said transition point of a value of said output data.

48. The apparatus for testing a semiconductor device as claimed in claim 47, wherein said judging unit judges quality of said semiconductor device further based on existence of said glitch detected by said glitch detector.

49. The apparatus for testing a semiconductor device as claimed in claim 47, wherein said glitch detector judges that there is said glitch of said output data if said transition points of a value of said output data detected by said transition point detector are more than or equal to two.

50. The apparatus for testing a semiconductor device as claimed in claim 47, wherein the apparatus further comprises a memory and stores a result of the glitch detector in the memory in association with said transition point of a value of said output data.

51. The apparatus for testing a semiconductor device as claimed in claim 45, wherein said reference phase measuring unit comprises:

means for generating a second multi-strobe having a plurality of strobes, of which phases are different by a small amount, in regard to said reference clock;

means for detecting said transition point of a value of said reference clock based on said second multi-strobe; and

means for calculating said output timing of said reference clock based on a strobe number of said second multi-strobe, in which said transition point of a value of said reference clock is detected.

52. The apparatus for testing a semiconductor device as claimed in claim 51, wherein said reference phase memory stores said strobe number of said second multi-strobe, in which said transition point of a value of said reference clock is detected.

53. The apparatus for testing a semiconductor device as claimed in claim 52, wherein said first multi-strobe generator sets a phase of said first multi-strobe based on said strobe number of said second multi-strobe stored by said reference phase memory.

54. The apparatus for testing a semiconductor device as claimed in claim 45, wherein said first multi-strobe generator comprises a plurality of delay devices connected in cascade, supplies a strobe to said plurality of delay devices connected in cascade, and generates said first multi-strobe based on strobes delayed respectively and outputted by said plurality of delay devices.

* * * * *

AMENDMENTS TO THE CLAIMS

Please amend the claims as follows.

1. (currently amended) An apparatus for testing a semiconductor device based on output data of said semiconductor device, comprising:

    a multi-strobe generator ~~for~~ configured to generat~~ing~~e a multi-strobe having a plurality of strobes, of which phases are different by a small amount;

    an output data transition point detector ~~for~~ configured to detect~~ing~~ a timing of rising or falling of a waveform of said output data based on said multi-strobe;

    a reference clock transition point detector ~~for~~ configured to detect~~ing~~ a timing of rising or falling of a reference clock outputted by said semiconductor device accompanying said output data, wherein said reference clock is a signal to set a timing of passing said output data, based on said multi-strobe; ~~and~~

    a judging unit ~~for~~ configured to judg~~eing~~ quality of said semiconductor device based on said timing of a timing of rising or falling of a waveform of said output data detected by said output data transition point detector and said timing of rising or falling of a waveform of said reference clock detected by said reference clock transition point detector; and

    <u>a glitch detector configured to detect existence of a glitch in regard to said output data based on said timing of rising or falling of a waveform of said output data detected by said output data transition point detector.</u>

2. (currently amended) ~~An~~ The apparatus for testing a semiconductor device as claimed in claim 1, wherein said judging unit judges quality of said semiconductor device based on whether or not a phase difference between said timing of rising or falling of a waveform of said output data detected by said output data transition point detector and said timing of rising or falling of a waveform of said reference clock detected by said reference clock transition point detector is within a predetermined range.

3. (currently amended) ~~An~~ The apparatus for testing a semiconductor device as claimed in claim 1, wherein said multi-strobe generator generates a first multi-strobe in order to detect a transition point of a value of said output data and a second multi-strobe in order to detect a transition point of a value of said reference clock.

4. (currently amended) ~~An~~ The apparatus for testing a semiconductor device as claimed in claim 3, further comprising a level comparator ~~for~~ configured to change~~ing~~ said output data and said reference clock into digital data represented by H logic or L logic, wherein

said output data transition point detector detects a value of said output data changed into said digital data in regard to a phase of each of strobes of said first multi-strobe, and if a value of said output data in regard to a phase of a first strobe of said first multi-strobe and a value of said output data in regard to a phase of a second strobe adjacent to said first strobe are different then determines said phase of said first strobe as said transition point of said value of said output data,

said reference clock transition point detector detects a value of said reference clock changed into said digital data in regard to a phase of each of strobes of said second multi-strobe, and if a value of said reference clock in regard to a phase of a third strobe of said second multi-strobe and a value of said reference clock in regard to a phase of a fourth strobe adjacent to said third strobe are different then determines said phase of said third strobe as said transition point of said value of said reference clock, and

said judging unit judges quality of said semiconductor device based on said transition point of said value of said output data and said transition point of said value of said reference clock.

5. (currently amended) ~~An~~ The apparatus for testing a semiconductor device as claimed in claim 4, wherein said judging unit judges quality of said semiconductor device based on whether or not a difference between a strobe number of said first multi-strobe indicating which timing of a strobe of said first multi-strobe said output data transition point detector detects said transition point of a value of said output data and a strobe number of said second multi-strobe indicating which timing of a strobe of said second multi-strobe said reference

clock transition point detector detects said transition point of a value of said reference clock at is within a predetermined range.

6. (currently amended) ~~An~~ The apparatus for testing a semiconductor device as claimed in claim 4, wherein said judging unit comprises a memory ~~for~~ configured to stor~~eing~~ a reference table to set quality of said semiconductor device about a combination of said strobe number of said first multi-strobe, in which said transition point of a value of said output data is detected and said strobe number of said second multi-strobe, in which said transition point of a value of said reference clock is detected, and judges quality of said semiconductor device based on said reference table.

7. (currently amended) ~~An~~ The apparatus for testing a semiconductor device as claimed in claim 4, wherein said output data transition point detector comprises [[a]] means for detecting whether a value of digital data in regard to said transition point of a value of said output data changes from said H logic to said L logic or changes from said L logic to said H logic.

8. (currently amended) ~~An~~ The apparatus for testing a semiconductor device as claimed in claim 4, wherein said output data transition point detector takes a transition point of an earliest phase or a transition point of a latest phase as said transition point of a value of said output data if a plurality of said transition points of a value of said output data are detected.

9. (canceled)

10. (currently amended) ~~An~~ The apparatus for testing a semiconductor device as claimed in claim 1 [[9]], wherein said judging unit judges quality of said semiconductor device further based on existence of said glitch detected by said glitch detector.

11. (currently amended) ~~An~~ The apparatus for testing a semiconductor device as claimed in claim 1 [[9]], wherein said glitch detector detects existence of a glitch in regard to said output data based on said transition point of a value of said output data.

12. (currently amended) ~~An~~ The apparatus for testing a semiconductor device as claimed in claim 11, wherein said glitch detector judges that there is said glitch of said output data if said transition points of a value of said output data are more than or equal to two.

13. (currently amended) An The apparatus for testing a semiconductor device as claimed in claim 1, wherein said multi-strobe generator comprises a plurality of delay devices having different delay times, supplies a strobe to each of said plurality of delay devices and outputs a plurality of strobes, delayed to have a different time delay respectively and outputted by said plurality of delay devices, as said multi-strobe.

14. (currently amended) An The apparatus for testing a semiconductor device as claimed in claim 13 [[1]], wherein said multi-strobe generator comprises a plurality of delay devices connected in cascade, supplies a strobe to each of said plurality of delay devices connected in cascade and generates said multi-strobe based on strobes delayed respectively and outputted by said plurality of delay devices.

15. (currently amended) An apparatus for testing a semiconductor device based on output data of said semiconductor device, comprising:

a first multi-strobe generator for configured to generateing a first multi-strobe having a plurality of strobes, of which phases are different by a small amount in regard to said output data;

a reference phase measuring unit for configured to measureing an output timing being a timing of rising or falling of a waveform of a reference clock which is a signal to set a timing of passing said output data and is outputted by said semiconductor device accompanied by said output data;

a reference phase memory for configured to memorizeing said output timing;

a transition point detector for detecting a transition point of a value of said output data based on said first multi-strobe;

a phase difference measuring unit for configured to measureing a phase difference between said output timing and said transition point of a value of said output data; and

a judging unit for configured to judgeing quality of said semiconductor device based on said phase difference; and

a glitch detector configured to detect existence of a glitch in regard to said transition point of a value of said output data.

16. (currently amended) ~~An~~ The apparatus for testing a semiconductor device as claimed in claim 15, wherein said first multi-strobe generator comprises a plurality of delay devices connected in cascade, supplies a strobe to said plurality of delay devices connected in cascade, and generates said first multi-strobe based on strobes delayed respectively and outputted by said plurality of delay devices.

17. (currently amended) ~~An~~ The apparatus for testing a semiconductor device as claimed in claim 15, wherein said transition point detector comprises [[a]] means for changing said output data into digital data represented by H logic or L logic, and

said transition point detector detects a value of said output data in regard to a phase of each of strobes of said first multi-strobe, and if a value of digital data in regard to a phase of a first strobe of said first multi-strobe and a value of digital data in regard to a phase of a second strobe adjacent to said first strobe are different then determines said phase of said first strobe as said transition point of said value of said output data.

18. (currently amended) ~~An~~ The apparatus for testing a semiconductor device as claimed in claim 17, wherein said transition point detector comprises [[a]] means for detecting whether said value of digital data in regard to said transition point changes from said H logic to said L logic or changes from said L logic to said H logic.

19. (currently amended) ~~An~~ The apparatus for testing a semiconductor device as claimed in claim 18, wherein said transition point detector takes a transition point of an earliest phase or a transition point of a latest phase as said transition point of a value of said output data if a plurality of said transition points of a value of said output data is detected.

20. (currently amended) ~~An~~ The apparatus for testing a semiconductor device as claimed in claim 15, wherein said reference phase measuring unit comprises:

[[a]] means for generating a second multi-strobe having a plurality of strobes, of which phases are different by a small amount, in regard to said reference clock;

[[a]] means for detecting said transition point of a value of said reference clock based on said second multi-strobe; and

[[a]] means for calculating said output timing of said reference clock based on a strobe number of said second multi-strobe, in which said transition point of a value of said reference clock is detected.

21. (currently amended) An The apparatus for testing a semiconductor device as claimed in claim 20, wherein said reference phase memory stores said strobe number of said second multi-strobe, in which said transition point of a value of said reference clock is detected.

22. (currently amended) An The apparatus for testing a semiconductor device as claimed in claim 21, wherein said first multi-strobe generator sets a phase of said first multi-strobe based on said strobe number of said second multi-strobe stored by said reference phase memory.

23. (canceled)

24. (currently amended) An The apparatus for testing a semiconductor device as claimed in claim 15 [[23]], wherein said judging unit judges quality of said semiconductor device further based on existence of said glitch detected by said glitch detector.

25. (currently amended) An The apparatus for testing a semiconductor device as claimed in claim 15 [[23]], wherein said glitch detector judges that there is said glitch of said output data if said transition points of a value of said output data detected by said transition point detector are more than or equal to two.

26. (currently amended) A method for testing a semiconductor device based on output data of said semiconductor device, comprising:
    a first multi-strobe generating step of generating a first multi-strobe having a plurality of strobes, of which phases are different by a small amount, in regard to said output data;
    an output data transition point detecting step of detecting a timing of rising or falling of a waveform of said output data based on said first multi-strobe;
    a second multi-strobe generating step of generating a second multi-strobe having a plurality of strobes, of which phases are different by a small amount, in regard to a reference clock, which is a signal to set a timing of passing said output data,

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said reference clock being outputted by said semiconductor device accompanying said output data;

a reference clock transition point detecting step of detecting a timing of rising or falling of a waveform of said reference clock based on said second multi-strobe;

a judging step of judging quality of said semiconductor device based on said timing of rising or falling of a waveform of said output data detected in said output data transition point detecting step and said timing of rising or falling of a waveform of said reference clock detected in said reference clock transition point detecting step; ~~and~~

an outputting step of outputting said judging quality of said semiconductor device; and

a glitch detecting step of detecting existence of a glitch in regard to said output data based on said transition point of a value of said output data,

wherein said judging step judges quality of said semiconductor device further based on existence of said glitch detected in said glitch detecting step.

27. (canceled)

28. (currently amended) A method for testing a semiconductor device based on output data of said semiconductor device, comprising:

a reference phase measurement step of measuring an output timing of a reference clock, which is a signal to set a timing of passing said output data, said reference clock being outputted by said semiconductor device accompanying said output data;

a reference phase memorizing step of memorizing said output timing;

a first multi-strobe generating step of generating a first multi-strobe having a plurality of strobes, of which phases are different by a small amount, in regard to said output data;

an output data transition point detecting step of detecting said transition point of a value of said output data based on said first multi-strobe;

a phase difference measuring step of measuring a phase difference between said output timing and said transition point of a value of said output data;

a judging step of judging quality of said semiconductor device based on said phase difference; ~~and~~

an outputting step of outputting said judging quality of said semiconductor device; and
a glitch detecting step of detecting existence of a glitch in regard to said output data based on said transition point of a value of said output data.

29. (canceled)

30. (new) The apparatus for testing a semiconductor device as claimed in claim 1, wherein the apparatus further comprises a memory and stores a result of the glitch detector in the memory in association with said transition point of a value of said output data.

31. (new) The apparatus for testing a semiconductor device as claimed in claim 7, wherein the apparatus further comprises a memory and stores a result of the glitch detector in the memory in association with said transition point of a value of said output data.

32. (new) The apparatus for testing a semiconductor device as claimed in claim 15, wherein the apparatus further comprises a memory and stores a result of the glitch detector in the memory in association with said transition point of a value of said output data.

33. (new) The apparatus for testing a semiconductor device as claimed in claim 18, wherein the apparatus further comprises a memory and stores a result of the glitch detector in the memory in association with said transition point of a value of said output data.

34. (new) The apparatus for testing a semiconductor device as claimed in claim 26, wherein the apparatus further comprises a memory and stores a result of the glitch detector in the memory in association with said transition point of a value of said output data.

35. (new) The apparatus for testing a semiconductor device as claimed in claim 28, wherein the apparatus further comprises a memory and stores a result of the glitch detector in the memory in association with said transition point of a value of said output data.

36. (new) An apparatus for testing a semiconductor device based on output data of said semiconductor device, comprising:

a multi-strobe generator configured to generate a multi-strobe having a plurality of strobes, of which phases are different by a small amount;

an output data transition point detector configured to detect a timing of rising or falling of a waveform of said output data based on said multi-strobe;

a reference clock transition point detector configured to detect a timing of rising or falling of a reference clock outputted by said semiconductor device accompanying said output data, wherein said reference clock is a signal to set a timing of passing said output data, based on said multi-strobe;

a judging unit configured to judge quality of said semiconductor device based on said timing of a timing of rising or falling of a waveform of said output data detected by said output data transition point detector and said timing of rising or falling of a waveform of said reference clock detected by said reference clock transition point detector;

a level comparator configured to change said output data and said reference clock into digital data represented by H logic or L logic,

wherein said multi-strobe generator generates a first multi-strobe in order to detect a transition point of a value of said output data and a second multi-strobe in order to detect a transition point of a value of said reference clock,

wherein said output data transition point detector detects a value of said output data changed into said digital data in regard to a phase of each of strobes of said first multi-strobe, and if a value of said output data in regard to a phase of a first strobe of said first multi-strobe and a value of said output data in regard to a phase of a second strobe adjacent to said first strobe are different then determines said phase of said first strobe as said transition point of said value of said output data,

wherein said reference clock transition point detector detects a value of said reference clock changed into said digital data in regard to a phase of each of strobes of said second multi-strobe, and if a value of said reference clock in regard to a phase of a third strobe of said second multi-strobe and a value of said reference clock in regard to a phase of a fourth strobe adjacent to said third strobe are different then determines said phase of said third strobe as said transition point of said value of said reference clock,

wherein said judging unit judges quality of said semiconductor device based on said transition point of said value of said output data and said transition point of said value of said reference clock, and

wherein said output data transition point detector takes a transition point of an earliest phase or a transition point of a latest phase as said transition point of a value of said output data if a plurality of said transition points of a value of said output data are detected.

37. (new) The apparatus for testing a semiconductor device as claimed in claim 36, wherein said judging unit judges quality of said semiconductor device based on whether or not a phase difference between said timing of rising or falling of a waveform of said output data detected by said output data transition point detector and said timing of rising or falling of a waveform of said reference clock detected by said reference clock transition point detector is within a predetermined range.

38. (new) The apparatus for testing a semiconductor device as claimed in claim 36, wherein said judging unit judges quality of said semiconductor device based on whether or not a difference between a strobe number of said first multi-strobe indicating which timing of a strobe of said first multi-strobe said output data transition point detector detects said transition point of a value of said output data and a strobe number of said second multi-strobe indicating which timing of a strobe of said second multi-strobe said reference clock transition point detector detects said transition point of a value of said reference clock at is within a predetermined range.

39. (new) The apparatus for testing a semiconductor device as claimed in claim 36, wherein said judging unit comprises a memory configured to store a reference table to set quality of said semiconductor device about a combination of said strobe number of said first multi-strobe, in which said transition point of a value of said output data is detected and said strobe number of said second multi-strobe, in which said transition point of a value of said reference clock is detected, and judges quality of said semiconductor device based on said reference table.

40. (new) The apparatus for testing a semiconductor device as claimed in claim 36, wherein said output data transition point detector comprises means for detecting whether a value of digital

data in regard to said transition point of a value of said output data changes from said H logic to said L logic or changes from said L logic to said H logic.

41. (new) The apparatus for testing a semiconductor device as claimed in claim 40, wherein the apparatus further comprises a memory and stores a result of the glitch detector in the memory in association with said transition point of a value of said output data.

42. (new) The apparatus for testing a semiconductor device as claimed in claim 36, further comprising a glitch detector configured to detect existence of a glitch in regard to said output data based on said timing of rising or falling of a waveform of said output data detected by said output data transition point detector.

43. (new) The apparatus for testing a semiconductor device as claimed in claim 42, wherein said judging unit judges quality of said semiconductor device further based on existence of said glitch detected by said glitch detector.

44. (new) The apparatus for testing a semiconductor device as claimed in claim 42, wherein said glitch detector detects existence of a glitch in regard to said output data based on said transition point of a value of said output data.

45. (new) The apparatus for testing a semiconductor device as claimed in claim 44, wherein said glitch detector judges that there is said glitch of said output data if said transition points of a value of said output data are more than or equal to two.

46. (new) The apparatus for testing a semiconductor device as claimed in claim 42, wherein the apparatus further comprises a memory and stores a result of the glitch detector in the memory in association with said transition point of a value of said output data.

47. (new) The apparatus for testing a semiconductor device as claimed in claim 36, wherein said multi-strobe generator comprises a plurality of delay devices having different delay times, supplies a strobe to each of said plurality of delay devices and outputs a plurality of strobes, delayed to have a different time delay respectively and outputted by said plurality of delay devices, as said multi-strobe.

48. (new) The apparatus for testing a semiconductor device as claimed in claim 47, wherein said multi-strobe generator comprises a plurality of delay devices connected in cascade, supplies a strobe to each of said plurality of delay devices connected in cascade and generates said multi-strobe based on strobes delayed respectively and outputted by said plurality of delay devices.

49. (new) An apparatus for testing a semiconductor device based on output data of said semiconductor device, comprising:

a first multi-strobe generator configured to generate a first multi-strobe having a plurality of strobes, of which phases are different by a small amount in regard to said output data;

a reference phase measuring unit configured to measure an output timing being a timing of rising or falling of a waveform of a reference clock which is a signal to set a timing of passing said output data and is outputted by said semiconductor device accompanied by said output data;

a reference phase memory configured to memorize said output timing;

a transition point detector configured to detect a transition point of a value of said output data based on said first multi-strobe;

a phase difference measuring unit configured to measure a phase difference between said output timing and said transition point of a value of said output data; and

a judging unit configured to judge quality of said semiconductor device based on said phase difference,

wherein said transition point detector comprises means for changing said output data into digital data represented by H logic or L logic, and said transition point detector detects a value of said output data in regard to a phase of each of strobes of said first multi-strobe, and if a value of digital data in regard to a phase of a first strobe of said first multi-strobe and a value of digital data in regard to a phase of a second strobe adjacent to said first strobe are different then determines said phase of said first strobe as said transition point of said value of said output data,

wherein said transition point detector comprises means for detecting whether said value of digital data in regard to said transition point changes from said H logic to said L logic or changes from said L logic to said H logic, and

wherein said transition point detector takes a transition point of an earliest phase or a transition point of a latest phase as said transition point of a value of said output data if a plurality of said transition points of a value of said output data is detected.

50. (new) The apparatus for testing a semiconductor device as claimed in claim 49, wherein said first multi-strobe generator comprises a plurality of delay devices connected in cascade, supplies a strobe to said plurality of delay devices connected in cascade, and generates said first multi-strobe based on strobes delayed respectively and outputted by said plurality of delay devices.

51. (new) The apparatus for testing a semiconductor device as claimed in claim 49, wherein said reference phase measuring unit comprises:

    means for generating a second multi-strobe having a plurality of strobes, of which phases are different by a small amount, in regard to said reference clock;

    means for detecting said transition point of a value of said reference clock based on said second multi-strobe; and

    means for calculating said output timing of said reference clock based on a strobe number of said second multi-strobe, in which said transition point of a value of said reference clock is detected.

52. (new) The apparatus for testing a semiconductor device as claimed in claim 51, wherein said reference phase memory stores said strobe number of said second multi-strobe, in which said transition point of a value of said reference clock is detected.

53. (new) The apparatus for testing a semiconductor device as claimed in claim 52, wherein said first multi-strobe generator sets a phase of said first multi-strobe based on said strobe number of said second multi-strobe stored by said reference phase memory.

54. (new) The apparatus for testing a semiconductor device as claimed in claim 49, further comprising a glitch detector configured to detect existence of a glitch in regard to said transition point of a value of said output data.

55. (new) The apparatus for testing a semiconductor device as claimed in claim 54, wherein said judging unit judges quality of said semiconductor device further based on existence of said glitch detected by said glitch detector.

56. (new) The apparatus for testing a semiconductor device as claimed in claim 54, wherein said glitch detector judges that there is said glitch of said output data if said transition points of a value of said output data detected by said transition point detector are more than or equal to two.

57. (new) The apparatus for testing a semiconductor device as claimed in claim 54, wherein the apparatus further comprises a memory and stores a result of the glitch detector in the memory in association with said transition point of a value of said output data.

58. (new) The apparatus for testing a semiconductor device as claimed in claim 49, wherein the apparatus further comprises a memory and stores a result of the glitch detector in the memory in association with said transition point of a value of said output data.

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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

Page _1_ of _1_

PATENT NO.   :   7,283,920

APPLICATION NO. :   10/732,763

ISSUE DATE   :   October 16, 2007

INVENTOR(S)   :   Masaru Doi et al.

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Drawings:

In the drawings, sheet 24 of 28, figure number 25 is incorrect. Please replace the drawing with the replacement drawing enclosed.

In the Claims:

In Claim in claim 12, column 29, line 27, the word "An" should be deleted.

In Claim 21, column 31, line 4, the word "An" should be deleted.

In Claim 35, column 33, line 55, the word "whereiii" should be --**wherein**--.

In Claim 38, column 34, line 10, the word "riot" should be --**not**--.

In Claim 38, column 34, line 11, the word "astrobe" should be --**a strobe**--.

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